Digital Modulation ISM Band Transceiver IC

Preliminary Technical Data

ADF7025

FEATURES

Low power, Zero- IF RF transceiver
Frequency bands:
- **431 MHz to 478 MHz**
- **862 MHz to 956 MHz**

Data rates supported:
- **1.35 kbps to 384kbps, FSK/GFSK**

2.3 V to 3.6 V power supply
Programmable output power:
- **–16 dBm to +13 dBm in 0.3 dBm steps**

Receiver sensitivity:
- **–102.4 dBm at 64 kbps, FSK**
- **–100.6 dBm at 172.8kbps, FSK**
- **–96.3 dBm at 345.6 kbps, FSK**

Low power consumption:
- **19 mA in receive mode**
- **28 mA in transmit mode (10 dBm output)**

On-chip VCO and fractional-N PLL
On-chip 7-bit ADC and temperature sensor
Digital RSSI
Integrated TRx switch
Leakage current <1 µA in power-down mode

APPLICATIONS

Wireless audio/video
Remote control/security systems
Wireless metering
Keyless entry
Home automation

FUNCTIONAL BLOCK DIAGRAM

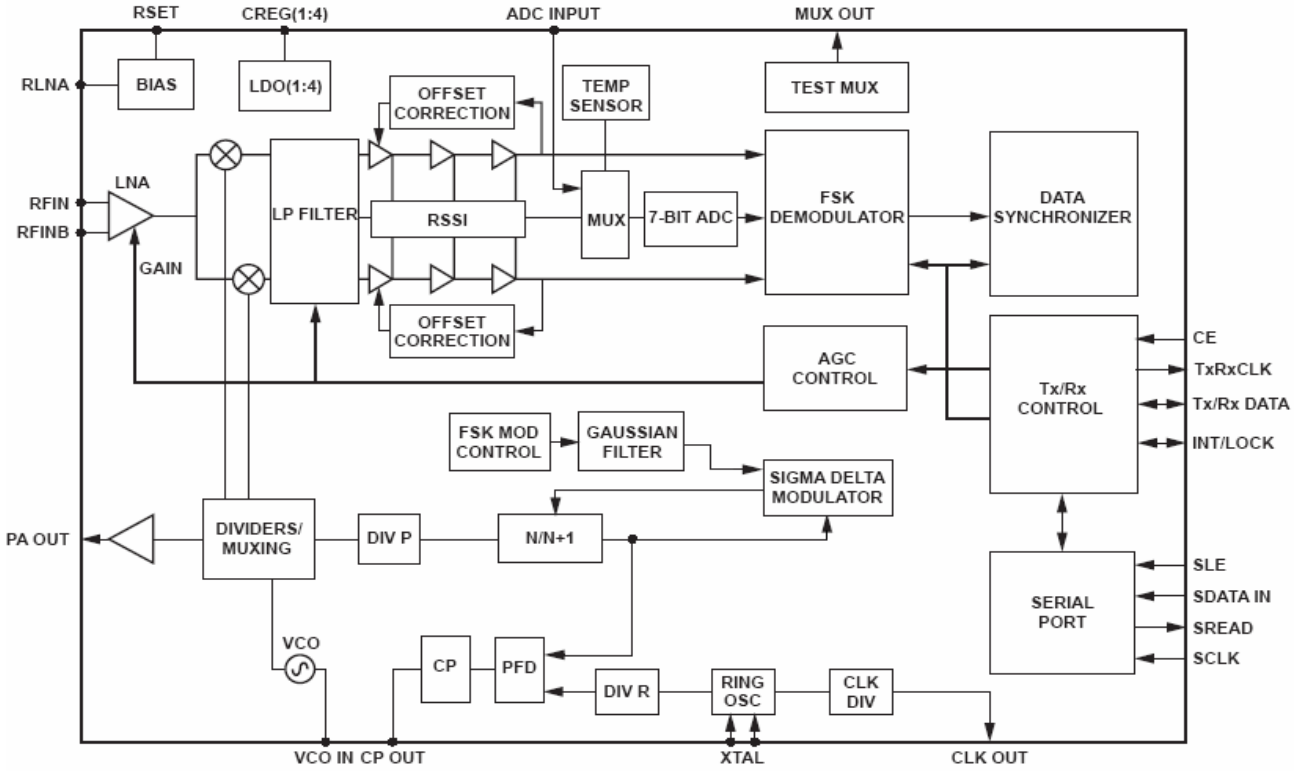

Figure 1.

Rev. PrC

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REVISION HISTORY

Revision PrC: Preliminary Version

GENERAL DESCRIPTION

The ADF7025 is a low power, highly integrated FSK/GFSK transceiver. It is designed for operation in the license–free ISM bands of 433MHz and 868MHz in Europe and 915MHz in North America. The ADF7025 is intended for applications operating under the European ETSI EN300-220 or the North American FCC (Part 15) regulatory standards. The ADF7025 is intended for wideband, high data rate applications with deviation frequencies from 80 kHz to 500 kHz and data rates from 1.35kbps to 384kbps. A complete transceiver can be built using a small number of external discrete components, making the ADF7025 very suitable for price-sensitive and area-sensitive applications.

The transmit section contains a VCO and low noise fractional-N PLL with output resolution of <1 ppm. The VCO operates at twice the fundamental frequency to reduce spurious emissions and frequency pulling problems.

The transmitter output power is programmable in 0.3 dB steps from −16 dBm to +13 dBm. The transceiver RF frequency, channel spacing, and modulation are programmable using a simple 3-wire interface. The device operates with a power supply range of 2.3 V to 3.6 V and can be powered down when not in use.

A zero-IF architecture is used in the receiver, minimizing power consumption and the external component count and avoiding the need for image rejection. The baseband filter has programmable bandwidths of ±300 kHz, ±450 kHz and ±600 kHz. A high pass pole at 80 kHz eliminates the problem of DC offsets that is characteristic of zero-IF architectures.

The ADF7025 supports a wide variety of programmable features including Rx linearity, sensitivity, and filter bandwidth, allowing the user to trade off receiver sensitivity and selectivity against current consumption, depending on the application.

An on-chip ADC provides readback of an integrated temperature sensor, an external analog input, the battery voltage, or the RSSI signal, which provides savings on an ADC in some applications. The temperature sensor is accurate to ±5°C over the full operating temperature range of −40°C to +8°C.

SPECIFICATIONS

V_{DD} = 2.3 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C. All measurements are performed using the EVAL-ADF7025EBX using PN9 data sequence, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
RF CHARACTERISTICS					
Frequency Ranges	862		956	MHz	
Frequency Ranges (Divide-by-2 Mode)	431		478	MHz	
Phase Frequency Detector Frequency	RF/256		20	MHz	
TRANSMISSION PARAMETERS					
Data Rate					
FSK/GFSK	1		384	kbps	
FSK/GFSK Frequency Deviation	100		311.89	kHz	PFD = 10 MHz
	100		796	kHz	PFD = 20 MHz
Deviation Frequency Resolution	220			Hz	PFD = 3.625 MHz
Gaussian Filter BT		0.5			
Modulation Index	1				
Transmit Power[1]	−20		+13	dBm	V_{DD} = 3.0 V, T_A = 25°C
Transmit Power Variation vs. Temp.		±1		dB	From −40°C to +85°C
Transmit Power Variation vs. VDD		±1		dB	From 2.3 V to 3.6 V at 915 MHz, T_A = 25°C
Transmit Power Flatness		±1		dB	From 902 MHz to 928 MHz, 3 V, T_A = 25°C
Programmable Step Size					
−20 dBm to +13 dBm		0.3125		dB	
Spurious Emissions during PLL Settling			−57	dBm	Mute PA until lock enabled (R2_DB5 = 1)
Integer Boundary		−55		dBc	50 kHz loop BW
Reference		−65		dBc	
Harmonics					
Second Harmonic		−27	−18	dBc	Unfiltered conductive
Third Harmonic		−21	−18	dBc	
All Other Harmonics			−35	dBc	
VCO Frequency Pulling		TBD		kHz rms	DR = 9.6 kbps
Optimum PA Load Impedance		39 + j61		Ω	FRF = 915 MHz
		48 + j54		Ω	FRF = 868 MHz
		54 + j94		Ω	FRF = 433 MHz
RECEIVER PARAMETERS					
FSK/GFSK Input Sensitivity					At BER = 1E − 3, FRF = 915 MHz, LNA and PA matched separately[2]
Sensitivity at 115.2 kbps		−102.6		dBm	FDEV = 100 kHz, LPF B/W = ±300kHz
Sensitivity at 172.8 kbps		−100.6		dBm	FDEV = 200 kHz, LPF B/W = ±450kHz
Sensitivity at 345.6 kbps		−96.3		dBm	FDEV = 300 kHz, LPF B/W = ±600kHz
Baseband Filter Bandwidths					Programmable
		±300		kHz	
		±450		kHz	
		±600		kHz	
LNA and Mixer, Input IP3					
Enhanced Linearity Mode		TBD		dBm	Pin = −20 dBm, 2 CW interferers
Low Current Mode		TBD		dBm	FRF = 915 MHz, f1 = FRF + 3 MHz
High Sensitivity Mode		TBD		dBm	F2 = FRF + 6 MHz, maximum gain
Rx Spurious Emissions[3]			TBD	dBm	<1 GHz at antenna input
			TBD	dBm	>1 GHz at antenna input
CHANNEL FILTERING					

Parameter	Min	Typ	Max	Unit	Test Conditions
Adjacent Channel Rejection (Offset = ±1 × IF Filter BW Setting)		TBD		dB	
Second Adjacent Channel Rejection (Offset = ±2 × IF Filter BW Setting)		TBD		dB	
Third Adjacent Channel Rejection (Offset = ±3 × IF Filter BW Setting)		TBD		dB	
Image Channel Rejection		TBD		dB	
CO-CHANNEL REJECTION		−2		dB	
Wide-Band Interference Rejection		70		dB	Swept from 100 MHz to 2 GHz, measured as channel rejection
BLOCKING:					Desired signal 3 dB above the input sensitivity level, CW interferer power level increased until BER = 10^{-2}
+/- 1MHz		TBD		dB	
+/- 5MHz		TBD		dB	
+/- 10MHz		TBD		dB	
+/- 10MHz (High Linearity Mode)		TBD		dB	
Saturation (Maximum Input Level)		12		dBm	FSK mode, BER = 10^{-3}
LNA Input Impedance		24 – j60		Ω	FRF = 915 MHz, RFIN to GND
		26 – j63		Ω	FRF = 868 MHz
		71 – j128		Ω	FRF = 433 MHz
RSSI					
Range at Input		−100 to −36		dBm	
Linearity		±2		dB	
Absolute Accuracy		±3		dB	
Response Time		150		µs	
PHASE-LOCKED LOOP					
VCO Gain		65		MHz/V	902 MHz to 928 MHz band, VCO adjust = 0, VCO_BIAS_SETTING = 8
		130		MHz/V	860 MHz to 870 MHz band, VCO adjust = 0
		65		MHz/V	433 MHz, VCO adjust = 0
Phase Noise (In-Band)		−89		dBc/Hz	PA = 0 dBm, V_{DD} = 3.0 V, PFD = 10 MHz, FRF = 915 MHz, VCO_BIAS_SETTING = 8
Phase Noise (Out-of-Band)		−110		dBc/Hz	1 MHz offset
Residual FM		128		Hz	From 200 Hz to 20 kHz, FRF = 868MHz
PLL Settling Time		40		µs	Measured for a 10 MHz frequency step to within 5 ppm accuracy, PFD = 20 MHz, LBW = 50kHz
REFERENCE INPUT					
Crystal Reference	3.625		24	MHz	
External Oscillator	3.625		24	MHz	
Load Capacitance		33		pF	
Crystal Start-Up Time		1.0		ms	Using 33 pF load capacitors
Input Level				CMOS levels	
TIMING INFORMATION					
Chip Enabled to Regulator Ready			TBD	µs	C_{REG} = 100 nF
Crystal Oscillator Startup Time		1		ms	With 19.2 MHz XTAL
Tx to Rx Turnaround Time		150 µs + (5 × T_{BIT})			Time to synchronized data, includes AGC settling.
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 × V_{DD}			V	
Input Low Voltage, V_{INL}			0.2 × V_{DD}	V	
Input Current, I_{INH}/I_{INL}			±1	µA	

Parameter	Min	Typ	Max	Unit	Test Conditions
Input Capacitance, C_{IN}			10	pF	
Control Clock Input			50	MHz	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	DV_{DD} − 0.4			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
CLK_{OUT} Rise/Fall			5	ns	
CLK_{OUT} Load			10	pF	
TEMPERATURE RANGE—T_A	−40		+85	°C	
POWER SUPPLIES					
Voltage Supply					
V_{DD}	2.3		3.6	V	All V_{DD} pins must be tied together
Transmit Current Consumption					FRF = 915 MHz, V_{DD} = 3.0 V, PA is matched in to 50 Ω
−20 dBm		14.6		mA	
−10 dBm		15.8		mA	
0 dBm		19.3		mA	
10 dBm		28		mA	
Receive Current Consumption					
Low Current Mode		19		mA	
High Sensitivity Mode		21		mA	
Power-Down Mode					
Low Power Sleep Mode		0.1	1	µA	

[1] Measured as maximum unmodulated power. Output power varies with both supply and temperature.
[2] Sensitivity for combined matching network case is typically 2 dB less than separate matching networks.
[3] Follow the matching and layout guidelines to achieve the relevant FCC/ETSI specifications.

TIMING CHARACTERISTICS

V_{DD} = 3 V ± 10%; VGND = 0 V, T_A = 25°C, unless otherwise noted.
Guaranteed by design, but not production tested.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	<10	ns	SDATA to SCLK Setup Time
t_2	<10	ns	SDATA to SCLK Hold Time
t_3	<25	ns	SCLK High Duration
t_4	<25	ns	SCLK Low Duration
t_5	<10	ns	SCLK to SLE Setup Time
t_6	<20	ns	SLE Pulse Width
t_7	<TBD	ns	SLE to SCLK Setup Time, Readback
t_8	<TBD	ns	SCLK to SREAD Data Valid, Readback
t_9	<TBD	ns	SREAD Hold Time after SCLK, Readback
t_{10}	<TBD	ns	SCLK to SLE Disable Time, Readback

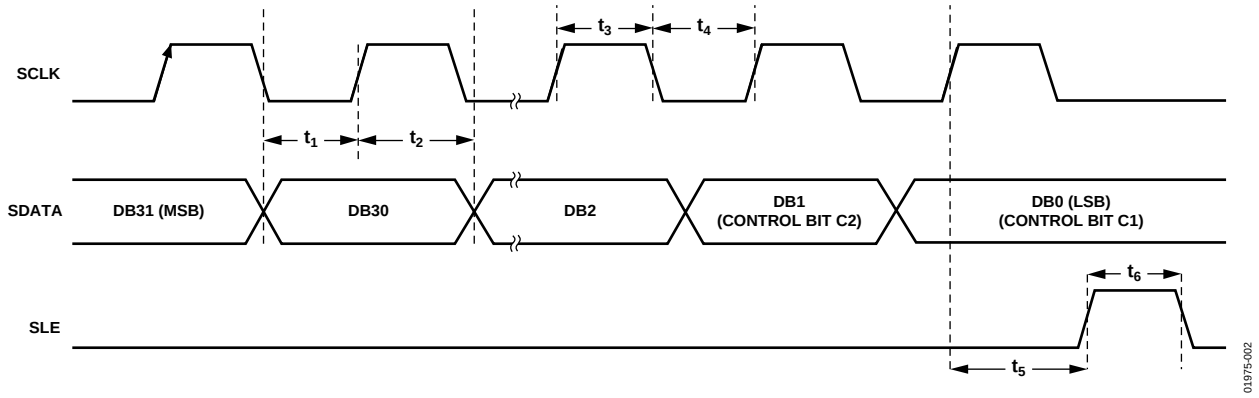

Figure 2. Serial Interface Timing Diagram

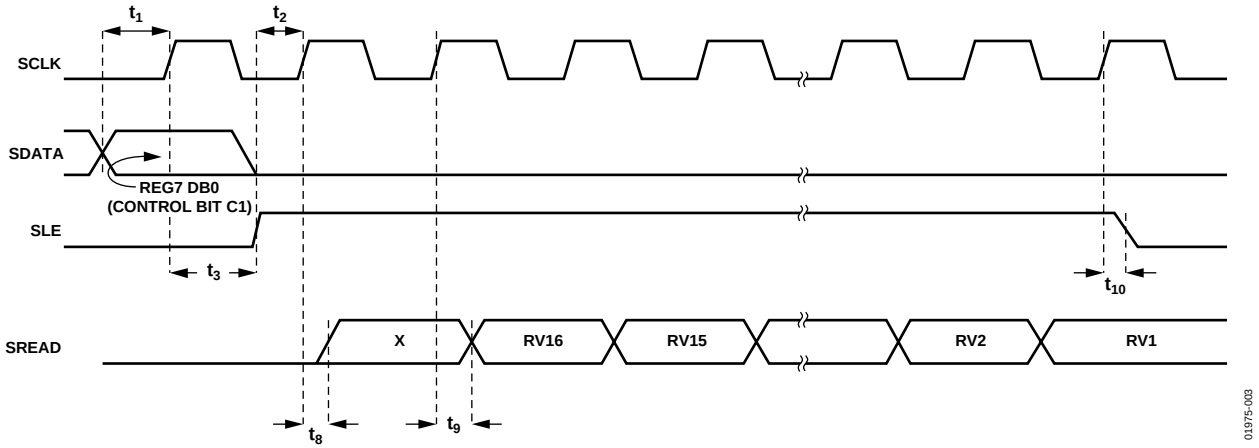

Figure 3. Readback Timing Diagram

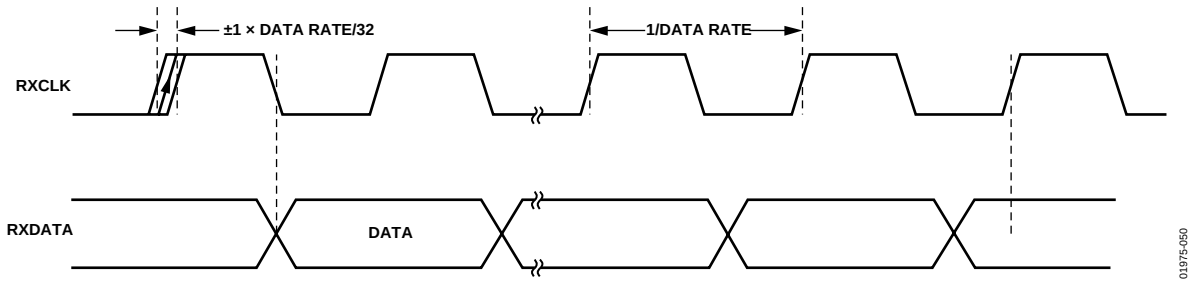

Figure 4. RxData/RxCLK Timing Diagram

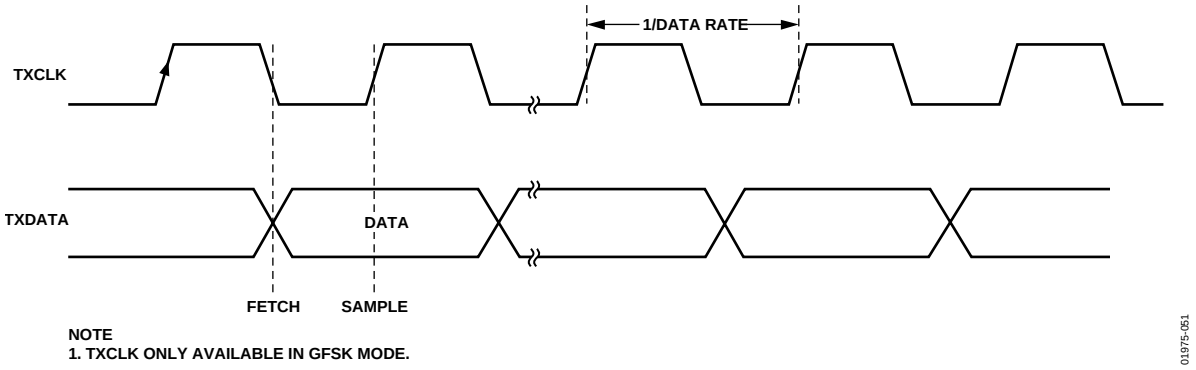

Figure 5. TxData/TxCLK Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND[1]	−0.3 V to +5 V
Analog I/O Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	125°C
MLF θ_{JA} Thermal Impedance	TBD°C/W
Lead Temperature Soldering	
Vapor Phase (60 s)	235°C
Infrared (15 s)	240°C

[1] GND = CPGND = RFGND = DGND = AGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high-performance RF integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

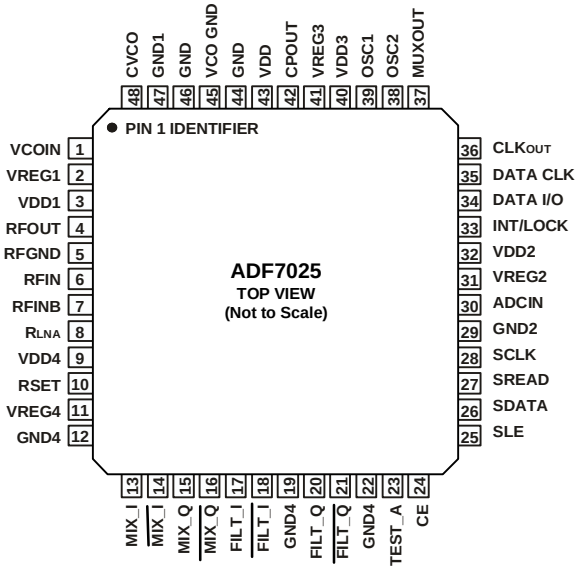

Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	VCOIN	The tuning voltage on this pin determines the output frequency of the voltage controlled oscillator (VCO). The higher the tuning voltage, the higher the output frequency.
2	VREG1	Regulator Voltage for PA Block. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
3	VDD1	Voltage Supply for PA Block. Decoupling capacitors of 0.1 µF and 10pF should be placed as close as possible to this pin. All VDD pins should be tied together.
4	RFOUT	The modulated signal is available at this pin. Output power levels are from −20 dBm to +13 dBm. The output should be impedance matched to the desired load using suitable components.
5	RFGND	Ground for Output Stage of Transmitter.
6	RFIN	LNA Input for Receiver Section. Input matching is required between the antenna and the differential LNA input to ensure maximum power transfer.
7	RFINB	Complementary LNA Input.
8	R_{LNA}	External bias resistor for LNA. Optimum resistor is 1.1 kΩ with 5% tolerance.
9	VDD4	Voltage supply for LNA/MIXER block. This pin should be decoupled to ground with a 10 nF capacitor.
10	RSET	External Resistor to Set Charge Pump Current and Some Internal Bias Currents. Use 3.6 kΩ with 5% tolerance.
11	VREG4	Regulator Voltage for LNA/MIXER block. A 100 nF capacitor should be placed between this pin and GND for regulator stability and noise rejection.
12	GND4	Ground for LNA/MIXER block.
13–18	MIX/FILT	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
19, 22	GND4	Ground for LNA/MIXER block.
20, 21, 23	FILT/TEST_A	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
24	CE	Chip Enable. Bringing CE low puts the ADF7025 into complete power-down. Register values are lost when CE is low, and the part must be reprogrammed once CE is brought high.
25	SLE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches. A latch is selected using the control bits.

Pin No.	Mnemonic	Function
26	SDATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This pin is a high impedance CMOS input.
27	SREAD	Serial Data Output. This pin is used to feed readback data from the ADF7025 to the microcontroller. The SCLK input is used to clock each readback bit (AFC, ADC readback) from the SREAD pin.
28	SCLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This pin is a digital CMOS input.
29	GND2	Ground for Digital Section.
30	ADCIN	Analog-to-Digital Converter Input. The internal 7-bit ADC can be accessed through this pin. Full scale is 0 to 1.9 V. Readback is made using the SREAD pin.
31	VREG2	Regulator Voltage for Digital Block. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
32	VDD2	Voltage Supply for Digital Block. A decoupling capacitor of 10 nF should be placed as close as possible to this pin.
33	INT/LOCK	Bidirectional Pin. In output mode (INTerrupt mode), the ADF7025 asserts the INT/ LOCK pin when it has found a match for the preamble sequence. In input mode (lock mode), the microcontroller can be used to lock the demodulator threshold when a valid preamble has been detected. Once the threshold is locked, NRZ data can be reliably received. In this mode, a demod lock can be asserted with minimum delay.
34	DATA I/O	Transmit Data Input/Received Data Output. This is a digital pin and normal CMOS levels apply.
35	DATA CLK	In receive mode, the pin outputs the synchronized data clock. The positive clock edge is matched to the center of the received data. In GFSK transmit mode, the pin outputs an accurate clock to latch the data from the microcontroller into the transmit section at the exact required data rate.
36	CLKOUT	A Divided-Down Version of the Crystal Reference with Output Driver. The digital clock output can be used to drive several other CMOS inputs such as a microcontroller clock. The output has a 50:50 mark-space ratio.
37	MUXOUT	This pin provides the Lock_Detect signal, which is used to determine if the PLL is locked to the correct frequency. Other signals include Regulator_Ready, which is an indicator of the status of the serial interface regulator.
38	OSC2	The reference crystal should be connected between this pin and OSC1. A TCXO reference can be used by driving this pin with CMOS levels and disabling the crystal oscillator.
39	OSC1	The reference crystal should be connected between this pin and OSC2.
40	VDD3	Voltage Supply for the Charge Pump and PLL Dividers. This pin should be decoupled to ground with a 0.01 µF capacitor.
41	VREG3	Regulator Voltage for Charge Pump and PLL Dividers. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
42	CPOUT	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
43	VDD	Voltage Supply for VCO Tank Circuit. This pin should be decoupled to ground with a 0.01 µF capacitor.
44–47	GND	Grounds for VCO Block.
48	CVCO	A 22 nF capacitor should be placed between this pin and VREG1 to reduce VCO noise.

OUTLINE DIMENSIONS

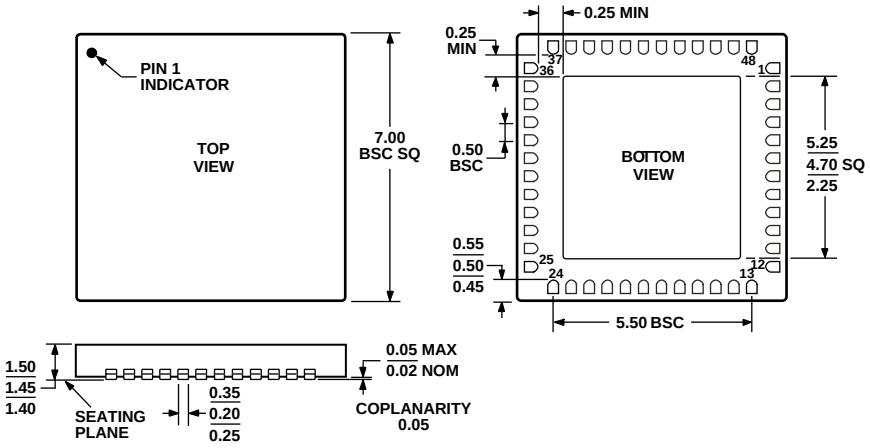

Figure 7. 48-Lead Lead Frame Chip Scale Package [MQ_LFCSP]
(CP-48-2)
7 mm × 7 mm Body, Thick Quad
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF7025BCP	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [MQ_LFCSP]	CP-48-2

NOTES

PR05542-0-4/05(PrC)